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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/810,499	03/19/2001	Harunobu Nakagawa	100353-00049	9664

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EXAMINER	
YOHA, CONNIE C	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/810,499	NAKAGAWA ET AL.	
	Examiner	Art Unit	
	Connie c. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,7 and 13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *4,7 and 13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The Amendment filed on 4/21/03 has been entered and are made of record.

2. Claims 4, 7, 13-16 are pending.

Response to Arguments

3. Applicant's arguments with respect to claims 4 and 7 have been considered but are moot in view of the new ground(s) of rejection due to the amended claims. Examiner uses new sited reference (Hazen et al, U.S. Pat. 5280447) to reject claim 4, 7 and 13-16.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 4 and 7 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Hazen et al, Pat. No. 5280447.

With regard to claim 4, Hazen discloses a semiconductor memory device, comprising: a plurality of input/output terminals (col. 4, line 55-58); a memory cell array (fig. 2, 52 and 51) which are divided into blocks (fig. 2, (100a-100n)-(115a-115n) of which belong to group 60a-60h and 61a-61h) (col. 6, line 43-57)), respectively corresponding to the input/ouput terminals such that that only one of the blocks

corresponds to a given one of the input/output terminals (col. 5, line 8-20); sense amplifiers, which are connected to the blocks at a side thereof, and amplify data o the memory cell array (fig, 2, SA0-SA15); switches which are respectively connected to the sense amplifiers (fig. 2, y-gating 56a-57h); and signal lines, which connected the sense amplifiers to a corresponding one of the input/output terminals via the switches (col. 7, line 65-col. 8, line 47), wherein said memory cell array includes flash memory cells, wherein data of the memory cell array is erased by one unit of erasure, wherein more than one but not all of said blocks are put together to form the unit of erasure (erasing block by block, each block is subdivided into sub-blocks, in another word, the memory array has total of (100a-100n)-(115a-115n) sub-blocks, one unit of erasure has 100a-100n sub-blocks, which is more than one blocks (100a-100n) but not all blocks(100a-100n)-(115a-115n) (also, col. 12, 17-46 and col. 15, line 5-16).

With regard to claim 7, Hazen discloses a semiconductor memory device which allows data of a plurality of pages to be read from a memory cell array and stored in sense amplifiers, and allow data of a selected gate to be read from the sense amplifiers and output to an exterior of the semiconductor memory device comprising: memory cell areas (fig. storing data to be input from and output to one common input/output terminal (fig. 2, (100a-100n)-(115a-115n) (col. 8, line 19-24), said memory cell areas respectively corresponding to the plurality of pages and provided adjacent to each other (fig. 2, 100a-115n), wherein the sense amplifiers corresponding to said memory cell areas are arranged adjacent to each other (fig. 2, SA0-SA15); and signal lines which connect the

sense amplifiers corresponding to said memory cell areas to the common input/output terminal (fig. 2, 64) (col. 8, line 19-24), wherein the memory cell array includes flash memory cells (col. 4, line 2-3), wherein data of said memory cell array is erased by one unit of erasure, wherein the unit of erasure is formed by putting together the memory cell areas for more than one but not all of input/output terminals (col. 15, line 5-52) (that is only i/o line connected to the sub-blocks of the selected blocks are subject to erase, the rest of the sub-blocks of the memory planes 51 and 52 are not subject to erase or are turn on).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hazen et al, Pat. No. 5280447 in view of Honda et al, Pat. No. 6377502.

With regard to claim 13, as applied in prior rejection, Hazen discloses all claimed subject matter except wherein each said unit of erasure is provided with a dedicated word-line driver. However, Honda discloses the use of a word line driver for each the unit of erasure (each core/block) (fig. 1, 2) for controlling the word line. Therefore, it would have been obvious for one having an ordinary skill in the art at the time the

invention was made to incorporate the use of a separate word-line driver for each of the unit of erasure of Hazen's as taught by Honda's device so as to control the word lines associated with the input/output section of the device (also with regard to claim 15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hazen et al, Pat. No. 5280447 in view of Liu, Pat. No. 6549474.

With regard to claim 14, as applied in prior rejection, Hazen discloses all claimed subject matter except wherein voltages necessary for erasure operation are generated by pump circuits, and said unit of erasure has a size commensurate with the capacity of the pump circuits. However, Liu discloses that voltages necessary for erasure operation can be generated by pump circuits (col. 1, line 32-36). Therefore, one having an ordinary skill in the art at the time the invention was made to a recognized that although silence, Hazen's erase voltages can be generated by pump circuits as taught by Liu, since it is well known and understood by those skilled in the art that in many electronic circuits, charge pump circuits are utilized to generate a positive pumped voltage that can be used to erase data stored in blocks of m5emory cells (col. 1, line 20-36) and that

erasing a plurality of blocks selected at the same time, the charge load capacity taken from the charge pump circuit of the erase voltage generating circuit varies depending on the sized of unit of erasure (also with regard to claim 16).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sakakibara et al (6466484) discloses FLASH memory device having unit of erasure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 306-5731. The

examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 4:30 PM. The examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

C.Yoha

June 2003